

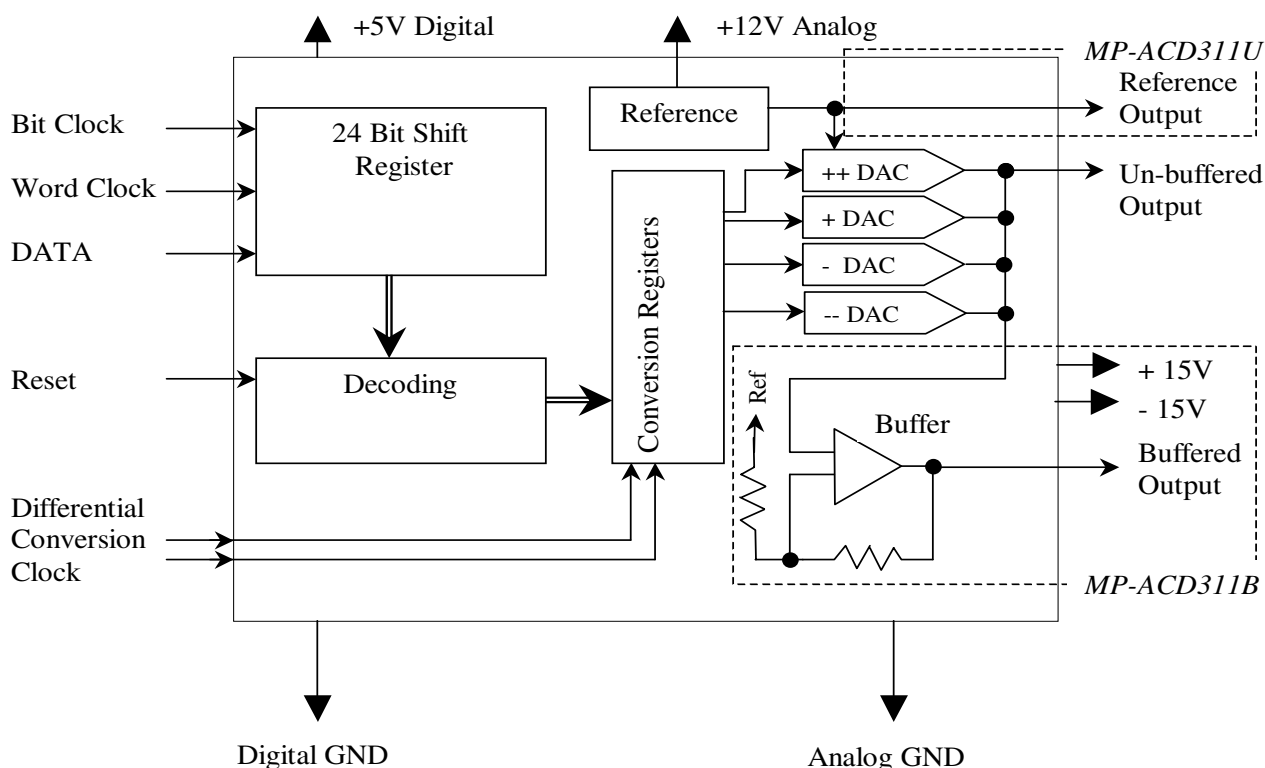
Features

- Designed specifically for high resolution digital audio
- True voltage output, no I/V converter required
- Low unbuffered output impedance 500 Ohms
- Built in high speed buffer (MP-ACD311B only)
- Ultra high dynamic range, 135 dB typical (<130dB guaranteed)
- 0Hz to 3.125MHz conversion rate (16x oversampling @ 192kHz or 8x @ 384 kHz)
- Integrated metal shield
- Low external parts count
- Custom grades and features available

Description

The MP-ACD311 is an ultra high performance 24 bit direct conversion audio DAC that provides unparalleled performance. The four-quadrant DAC architecture ensures the best possible performance for small and large signals without averaging (like a Delta-sigma data converter.) A fast conversion rate, low noise and distortion at all signal levels delivers the finest digital audio possible with a minimum of external components.

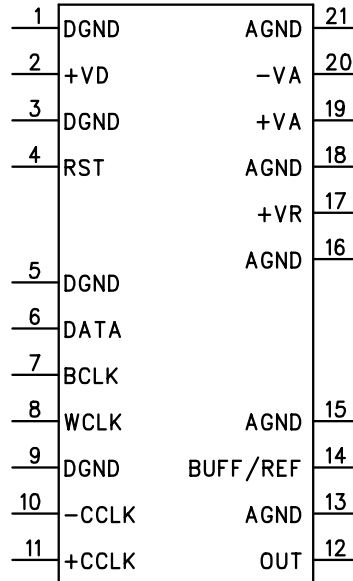
Offered with an internal buffer (MP-ACD311B) or without (MP-ACD311U.)



Specifications for MP-ACD311

All Specifications measured at 25°C, +VD = 5V, +VR = 12V, +VA = 12V, -VA = -12V, FS = 384KHz, Data = 24bit

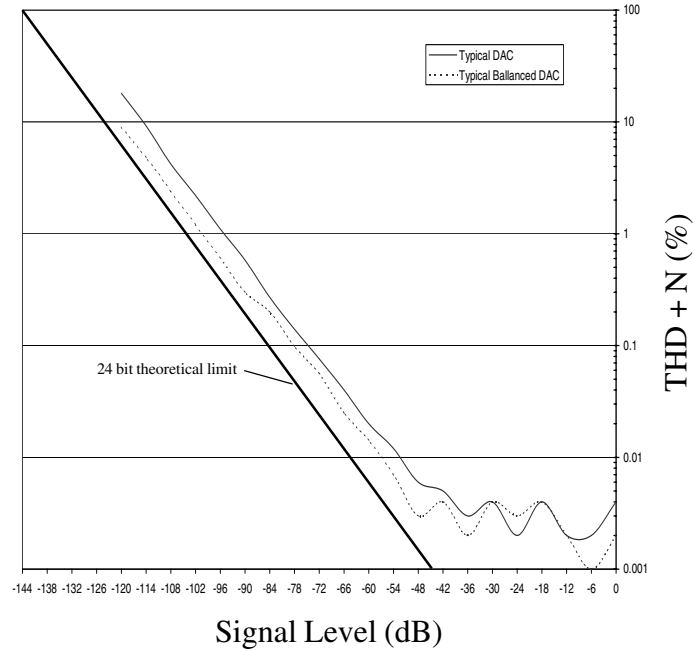
Parameter	Conditions	Minimum	Typical	Maximum	Units
Resolution			24		Bits
Data Format					
Audio Data Format		24-Bit, MSB First, Two's Complement			
Sampling Frequency		0		3125	KHz
Serial Clock Frequency				75	MHz
Digital Input	+VD = 5V				
Logic High Level		3.8		5.25	V
Logic Low Level		-0.25		1.6	V
Conversion Clock	+VR > 9V				
+CCLK Input Range		-0.25		5.25	V
-CCLK Input Range		-0.25		5.25	V
Analog Output					
Output Range (14)	Buffered	-5		5	V
Output Range (12)	Unbuffered	0		5	V
Output Current (14)	Buffered	-25		25	mA
Output Current (12)	Unbuffered	0		10	mA
Output Impedance (14)	Buffered		5		Ohm
Output Impedance (12)	Unbuffered		500		Ohm
Reference Out	MP-ACD311U	4.995	5.000	5.005	V
DC Accuracy					
Bipolar Zero Error (14)	Buffered	-5		5	mV
Bipolar Zero Error (12)	Unbuffered	-1		1	mV
Gain Error (14)	Buffered	0.8		0.8	% FSR
Gain Error (12)	Unbuffered	0.5		0.5	% FSR
Dynamic Performance					
THD+N 0dB			0.004	0.006	%
THD+N -60dB			0.02	0.03	%
Dynamic Range	A-weighted	130	135		dB
Signal to Noise Ratio	A-weighted	140	145		dB
Low Level Linearity	1KHz -90dB	-0.15		0.15	dB
Settling Time			100	150	ns
Power Requirements					
Positive Digital (+VD)		4.75	5.00	5.25	V
			24	50	mA
Positive Analog (+VR)		10	12	15	V
			38	44	mA
Positive Buffer (+VA)	MP-ACD311B	8	12	15	V
			10	35	mA
Negative Buffer (-VA)	MP-ACD311B	-15	-12	-8	V
		-35	-10		mA



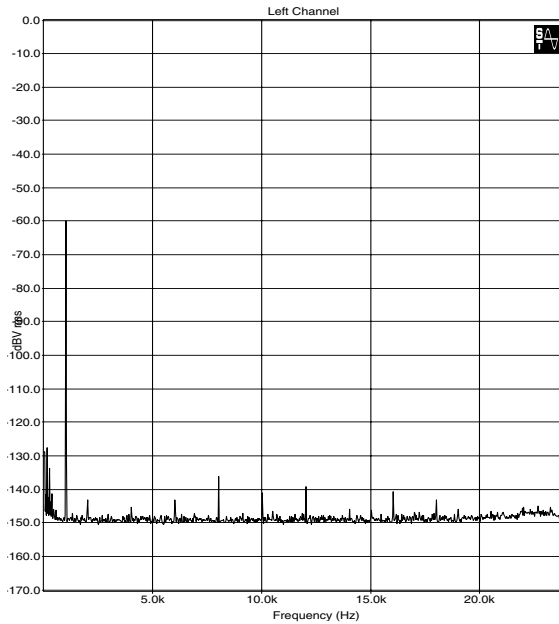
Pin Assignments for MP-ACD311

Pin Assignments are for all versions except where noted

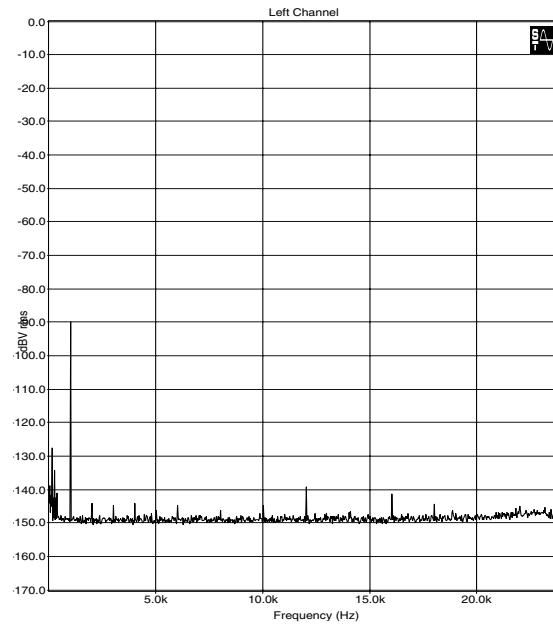
Pin #	Pin Name	Function
1	DGND	Digital Ground, connected internally to AGND
2	+VD	Digital Power Input, 5V supply
3	DGND	Digital Ground
4	RST	Shift Register Reset Input, Low = Reset, High = Shift
5	DGND	Digital Ground
6	DATA	Two's Complement Data Input 24-Bit, MSB First, Right Justified
7	BCLK	Bit Clock Input, Data is shifted on High to Low transition
8	WCLK	Word Frame Clock, Data is latched on High to Low transition
9	DGND	Digital Ground
10	-CCLK	½ DAC Conversion Clock Input, DAC converts on High to Low
11	+CCLK	½ DAC Conversion Clock Input, DAC converts on Low to High
12	OUT	Unbuffered Analog Output, 500 Ohm, 0V - 5V
13	AGND	Analog Ground, connected to DGND internally
14	BUFF/REF	MP-ACD311B = Buffered Analog Output MP-ACD311U = 5V Reference Output
15	AGND	Analog Ground
16	AGND	Analog Ground
17	+VR	Internal Reference Power Supply Input, 10V - 15V
18	AGND	Analog Ground
19	+VA	MP-ACD311B , Buffer Power Supply Input, 8V - 15V MP-ACD311U , No Connection
20	-VA	MP-ACD311B , Buffer Power Supply Input, -8V - -15V MP-ACD311U , No Connection
21	AGND	Analog Ground



- 60 dB Dynamic Range FFT



-90 dB Dynamic Range FFT



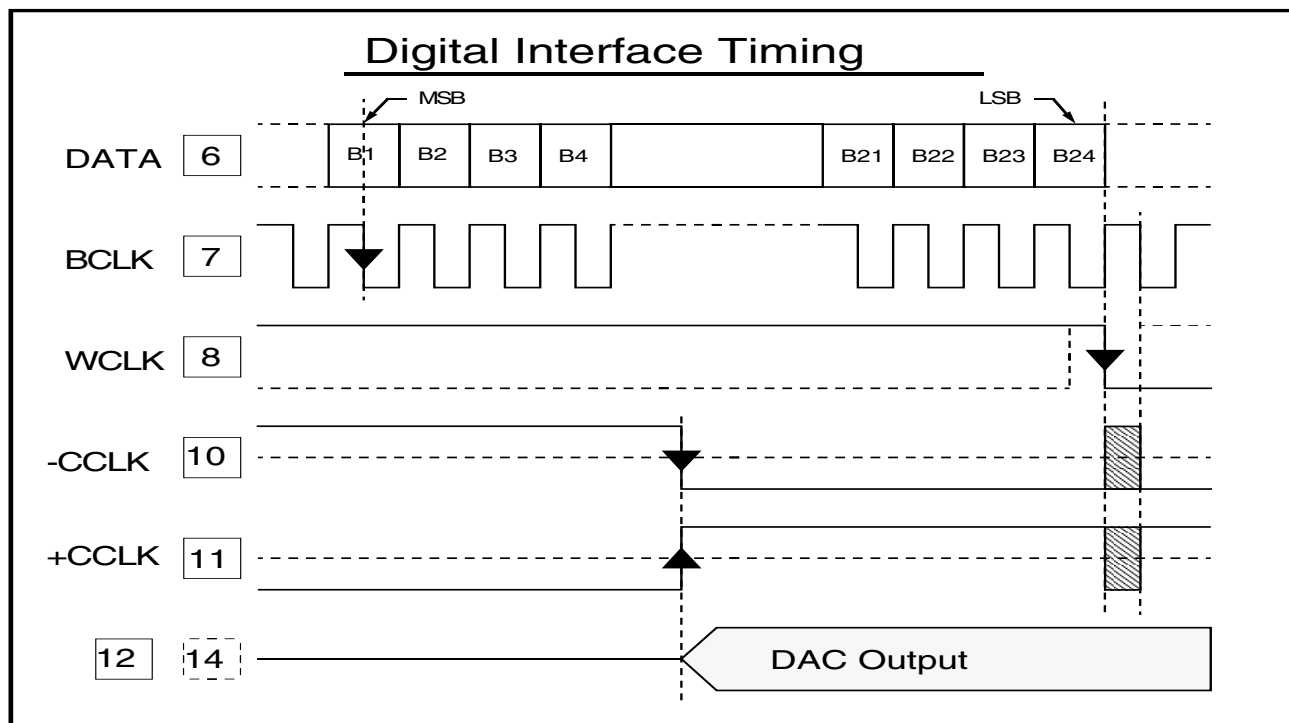
Data Interface

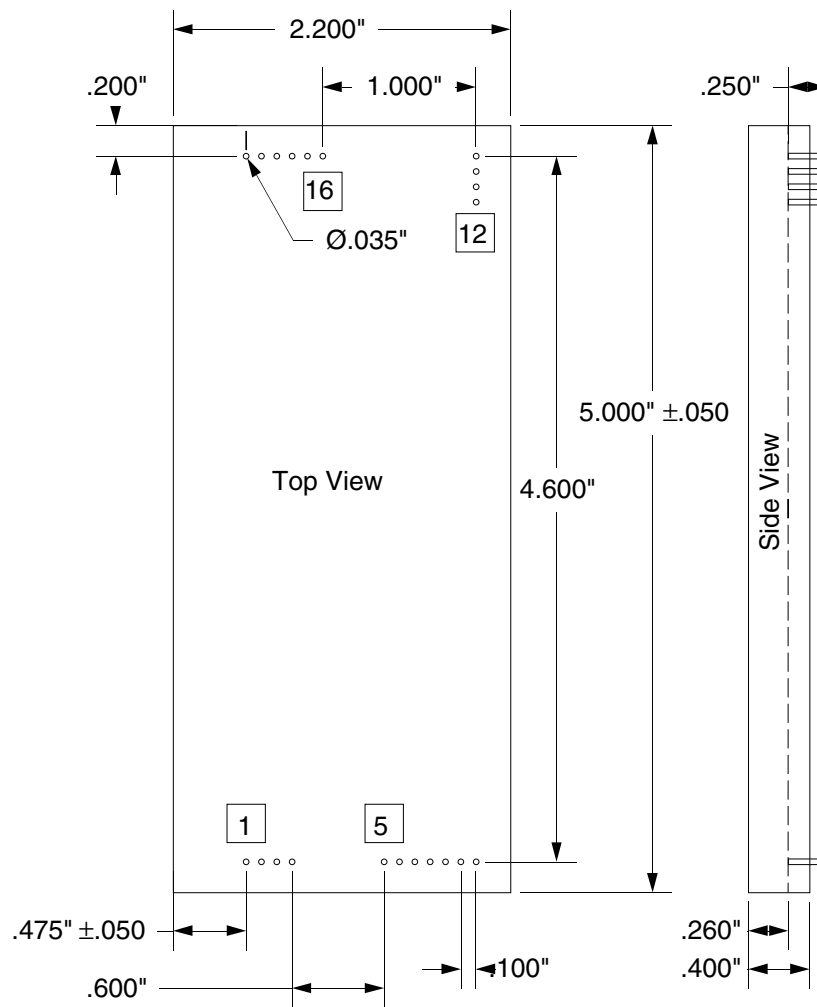
The audio data interface is designed for simple connection to most digital filters. A two's complement data coding scheme was chosen for ease in digital signal inversion (only one inverter is required) and digital muting (an all high or low data signal will produce an output within 1 LSB of Bipolar Zero.) Data is presented to the DATA (6) pin serially. After a setup time of 3 ns (min) the falling edge of BCLK (7) shifts the data into the internal shift register. 24 cycles or more of BCLK (7) are required per frame to shift the data into the proper position, less than 24 cycles of BCLK (7) during one frame will cause the new data to be misaligned and a portion of the previous data will not be cleared causing erroneous data to be presented for decoding. After the last falling edge (5 ns min) of BCLK (7) in a frame the falling edge of WCLK (8) latches the data for decoding. Immediately after the high to low transition of WCLK (8) internal decoding takes place, during the 20ns after the high to low transition of WCLK (8) the data presented to the DAC is in an indeterminate state. If a conversion (a high to low transition of -CCLK (10)) is initiated during this interval an erroneous output will occur.

To combat conversion period instability (jitter) a separate differential clock (CCLK) input is provided for conversion. CCLK may transition asynchronously from all other signals provided that it does not initiate a conversion within the 20ns after a high to low transition of WCLK (8). CCLK is the input of an ultra high-speed comparator allowing compatibility with CMOS, TTL, LVCMOS, PECL or LVDS clock signals. Non-differential signals will require a threshold to be set for the unused input, a divider between ground and power with a bypass capacitor is recommended.

Reset RST (4) asynchronously clears the contents of the shift register to zero, this is presented for decoding on the next falling WCLK (8) and present at the DACs output on the following conversion clock.

Two's Complement Coding	
100000000000000000000000	Positive Full Scale
111111111111111111111110	Zero +2LSB
111111111111111111111111	Zero +1LSB
000000000000000000000000	Bipolar Zero
000000000000000000000001	Zero -1LSB
011111111111111111111111	Negative Full Scale





MSB Technology DAC Module

Circuit Example

The circuit below shows the typical connections for this DAC module. MSB typically recommends a high oversampling ratio digital filter without analog filtering as shown below. An analog reconstruction filter may be added if desired for reduced high frequency energy or for use as a non-oversampling DAC. The MP-ACD311B contains an internal buffer while the MP-ACD311U provides a low impedance reference out for easy DC restoration without a servo.

